DLD

EXPERIMENT – 10

Aim: To simulate the logic gates of 8bit shift registers

Tools used: vivado software

Truth table:

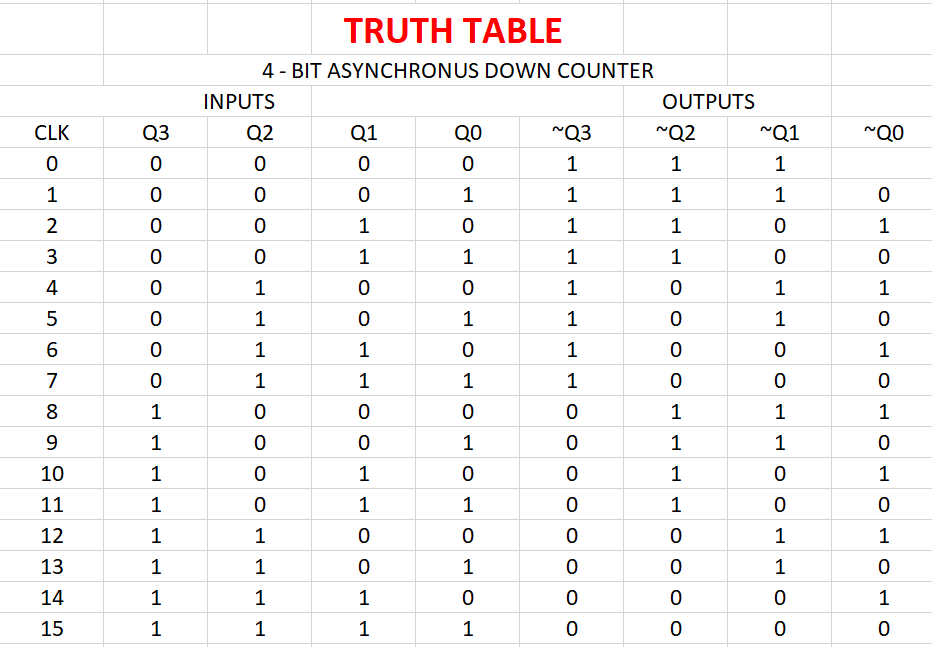
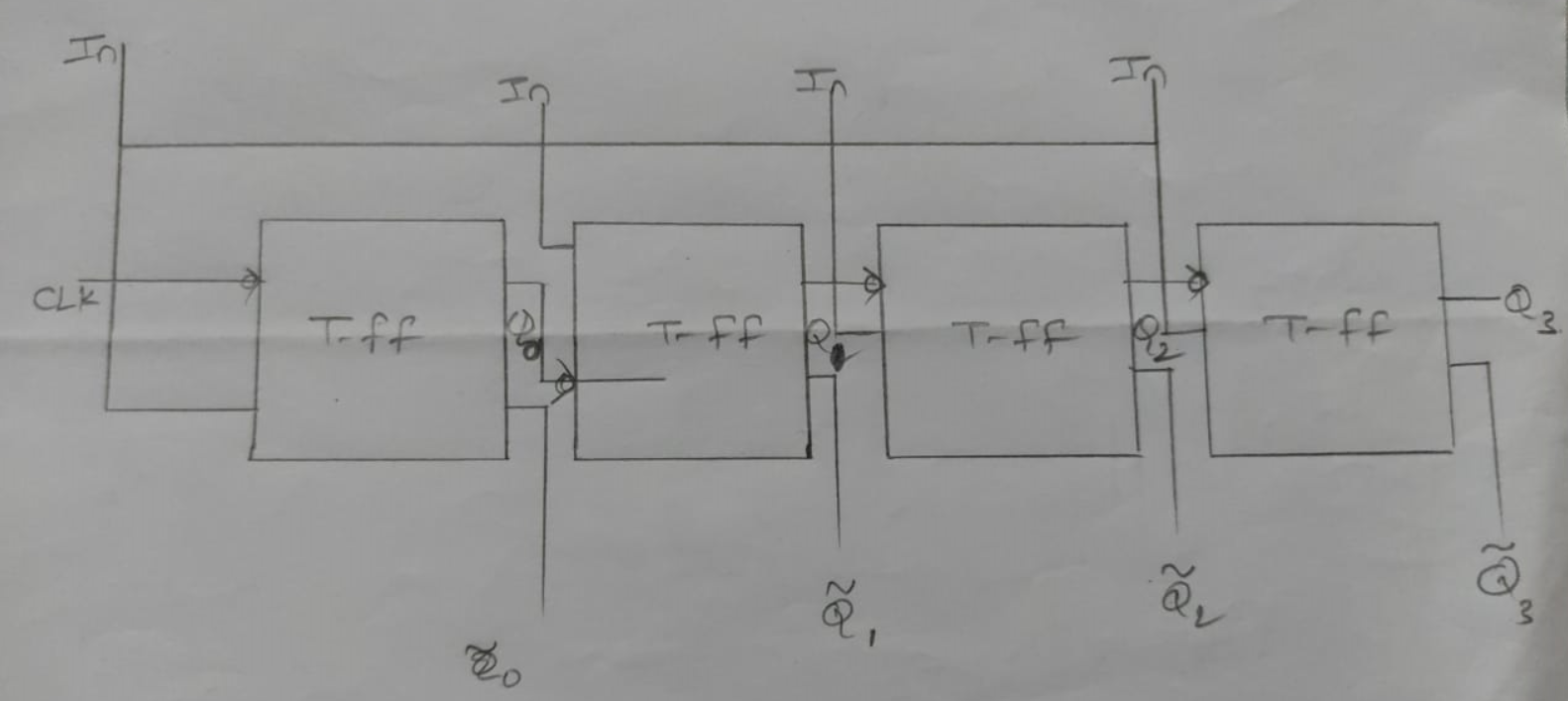
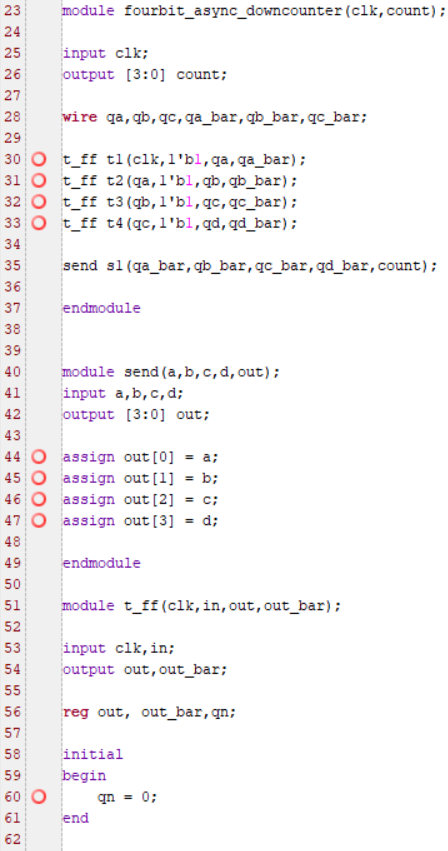
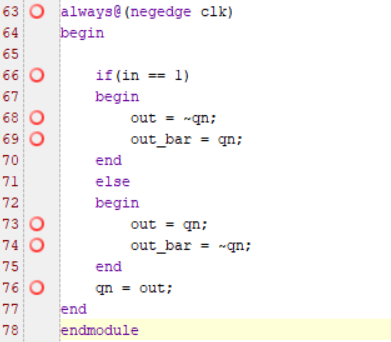


Diagram:

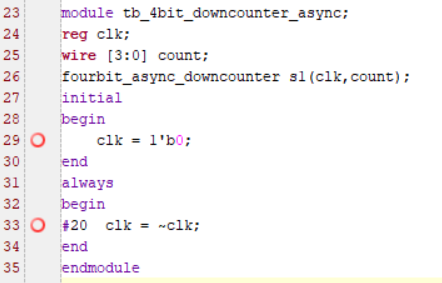


Verilog codes:

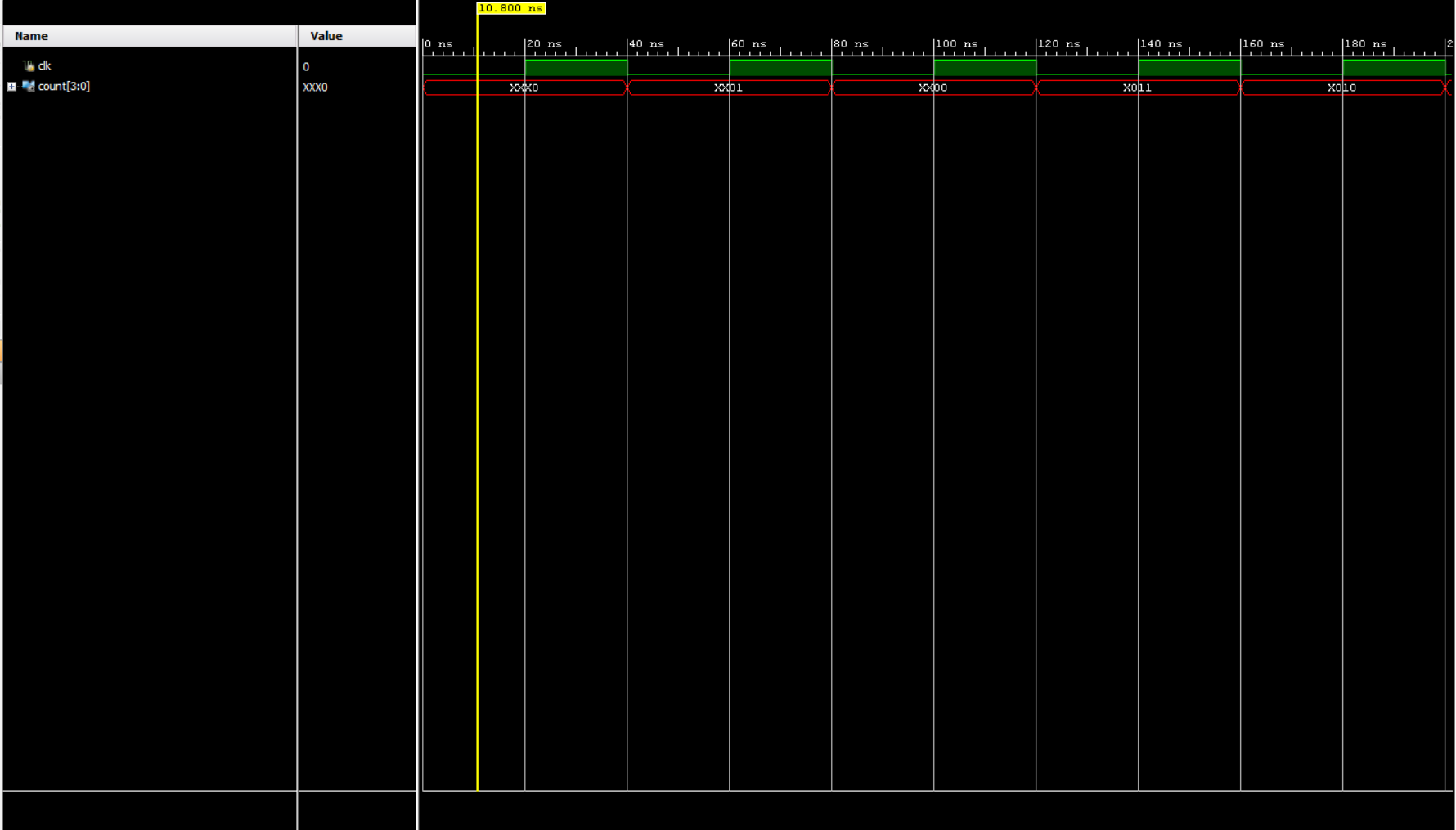


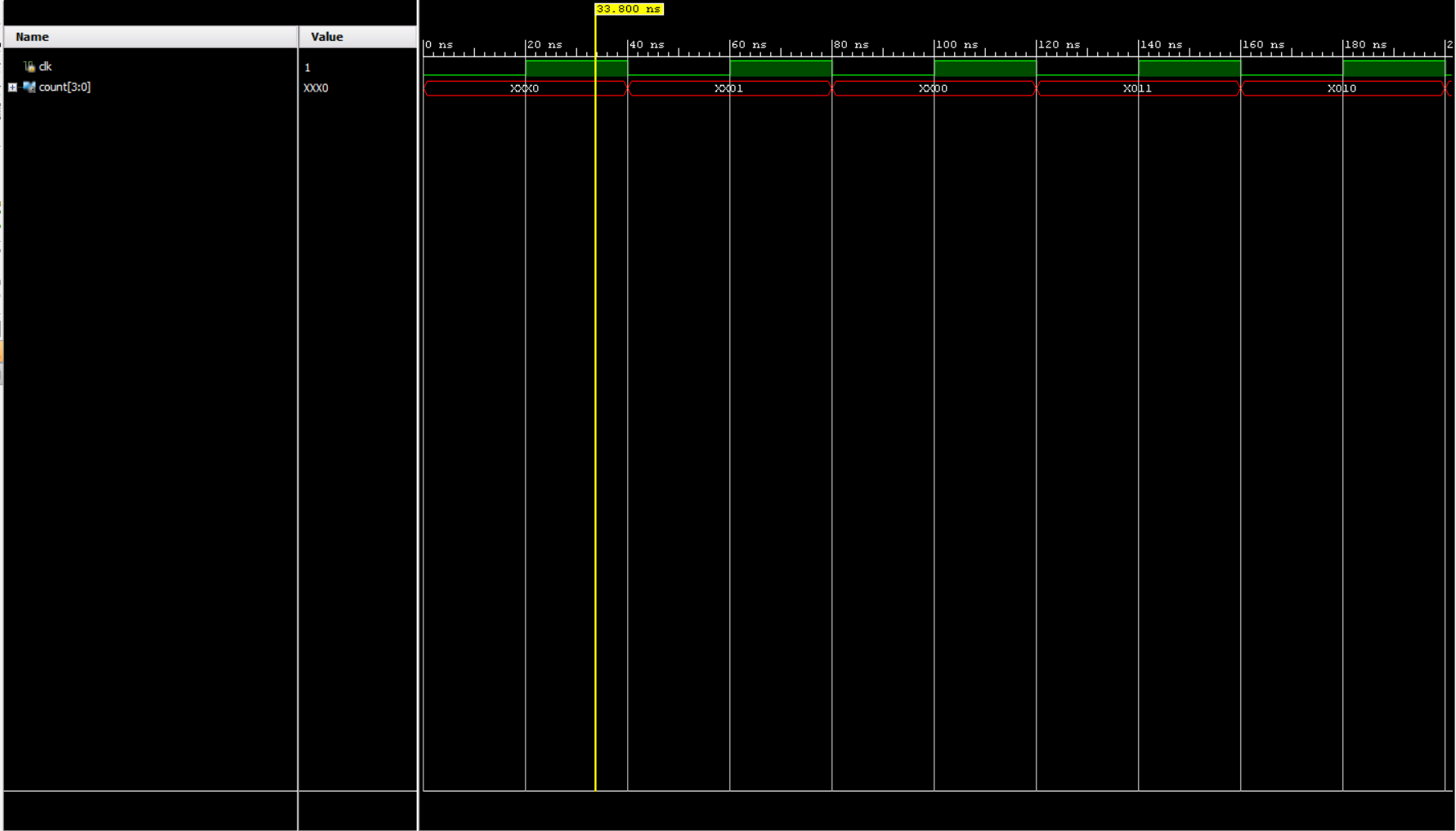


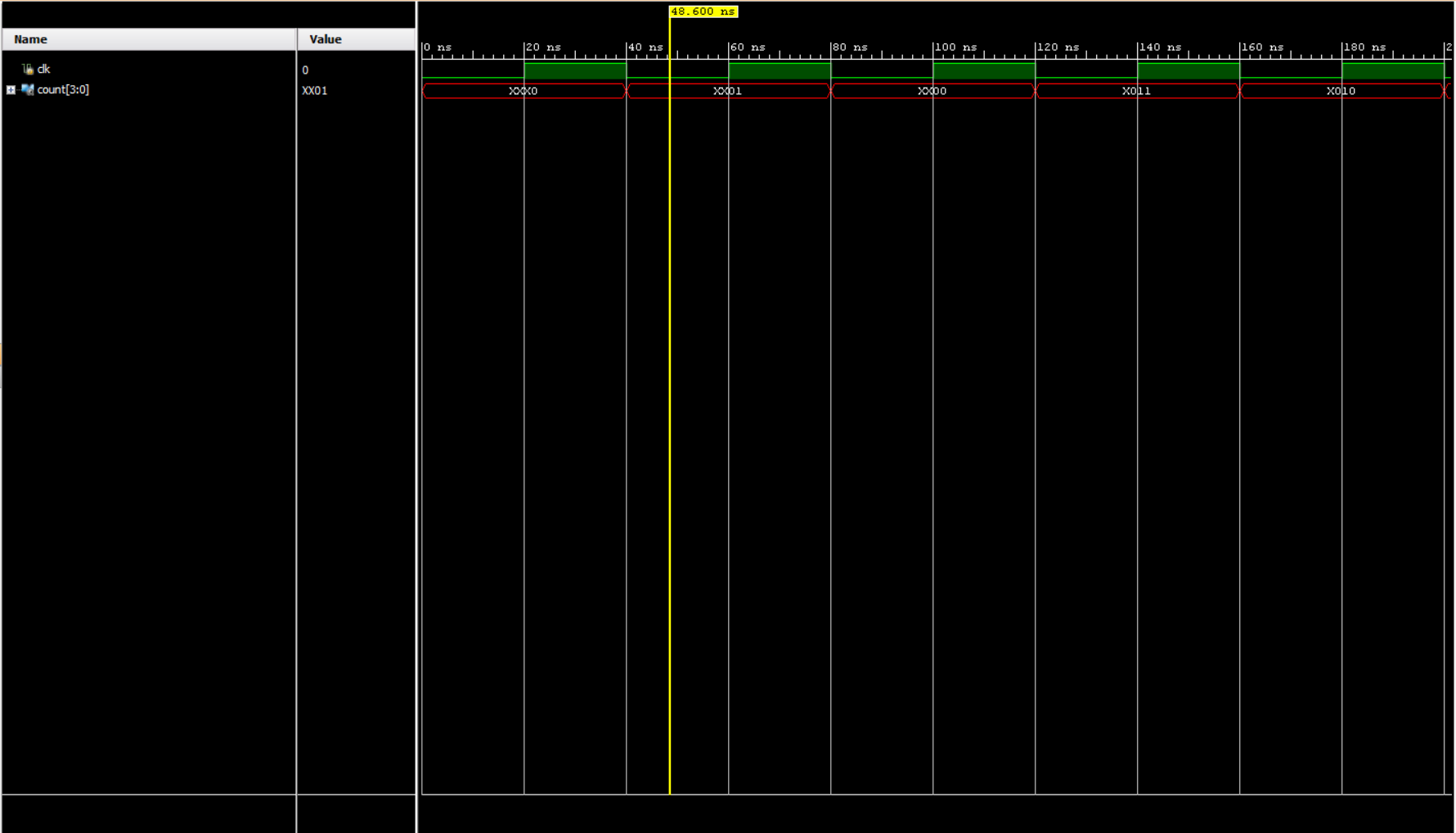
Test bench code:

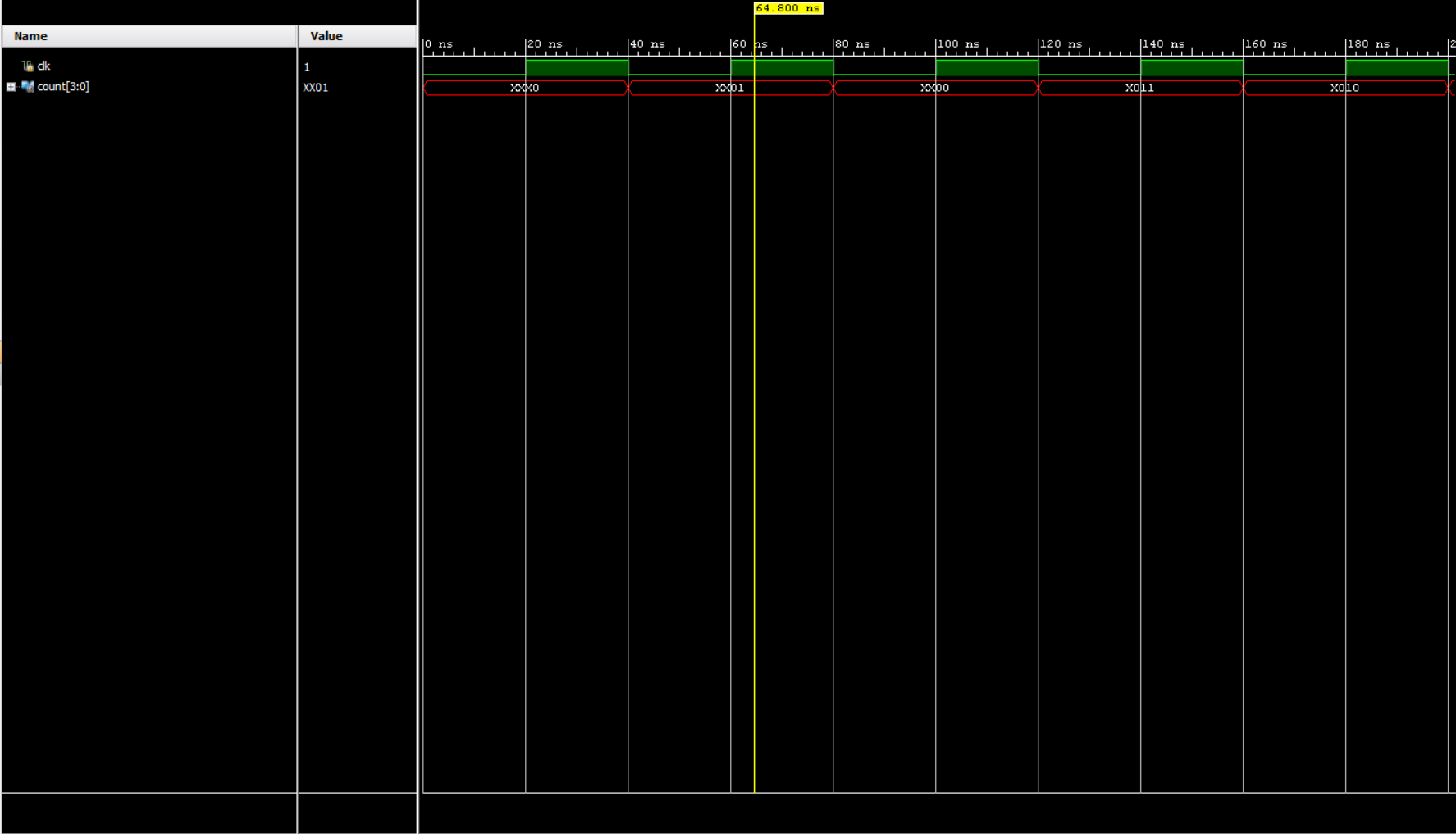


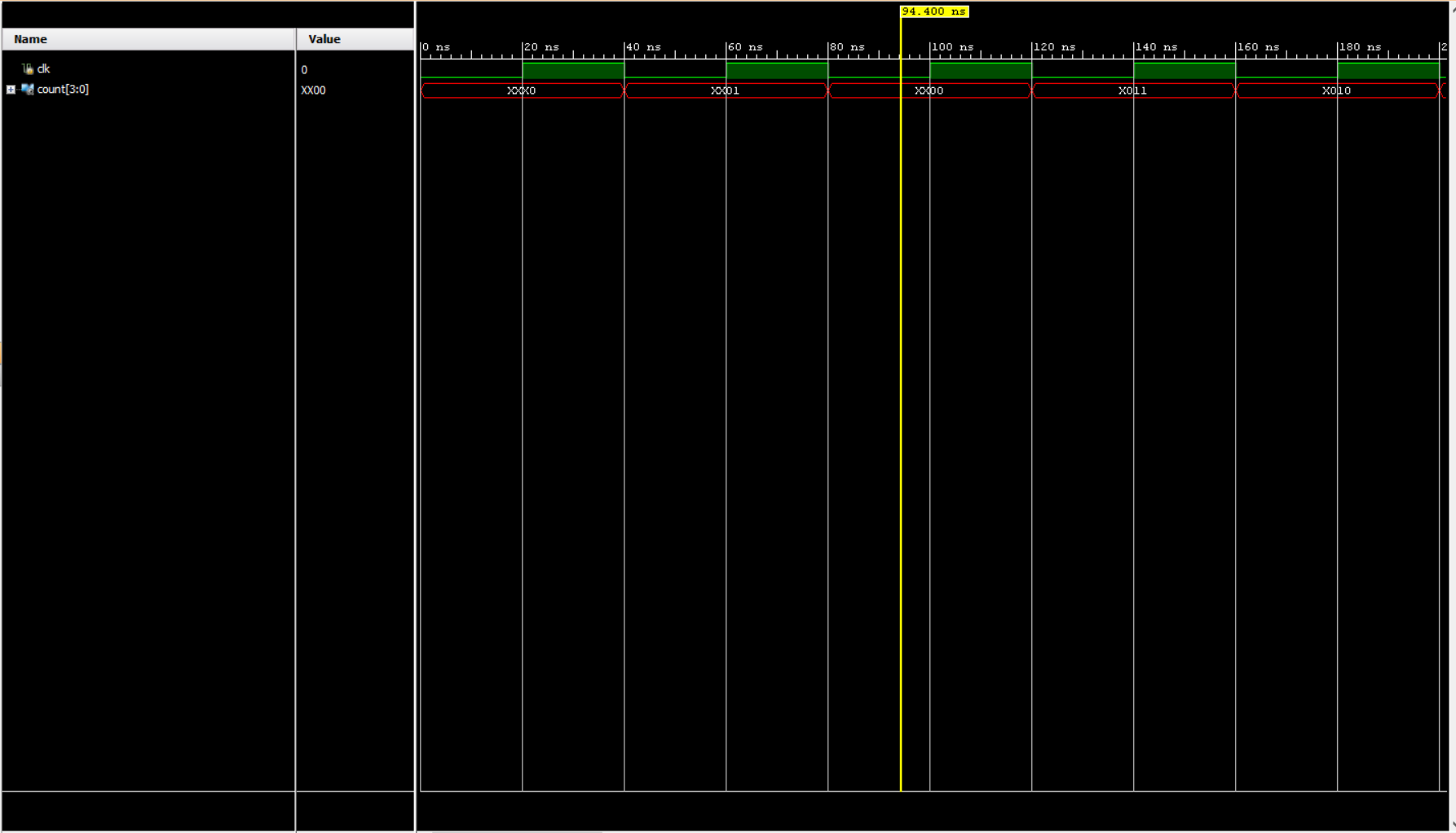
Outputs:



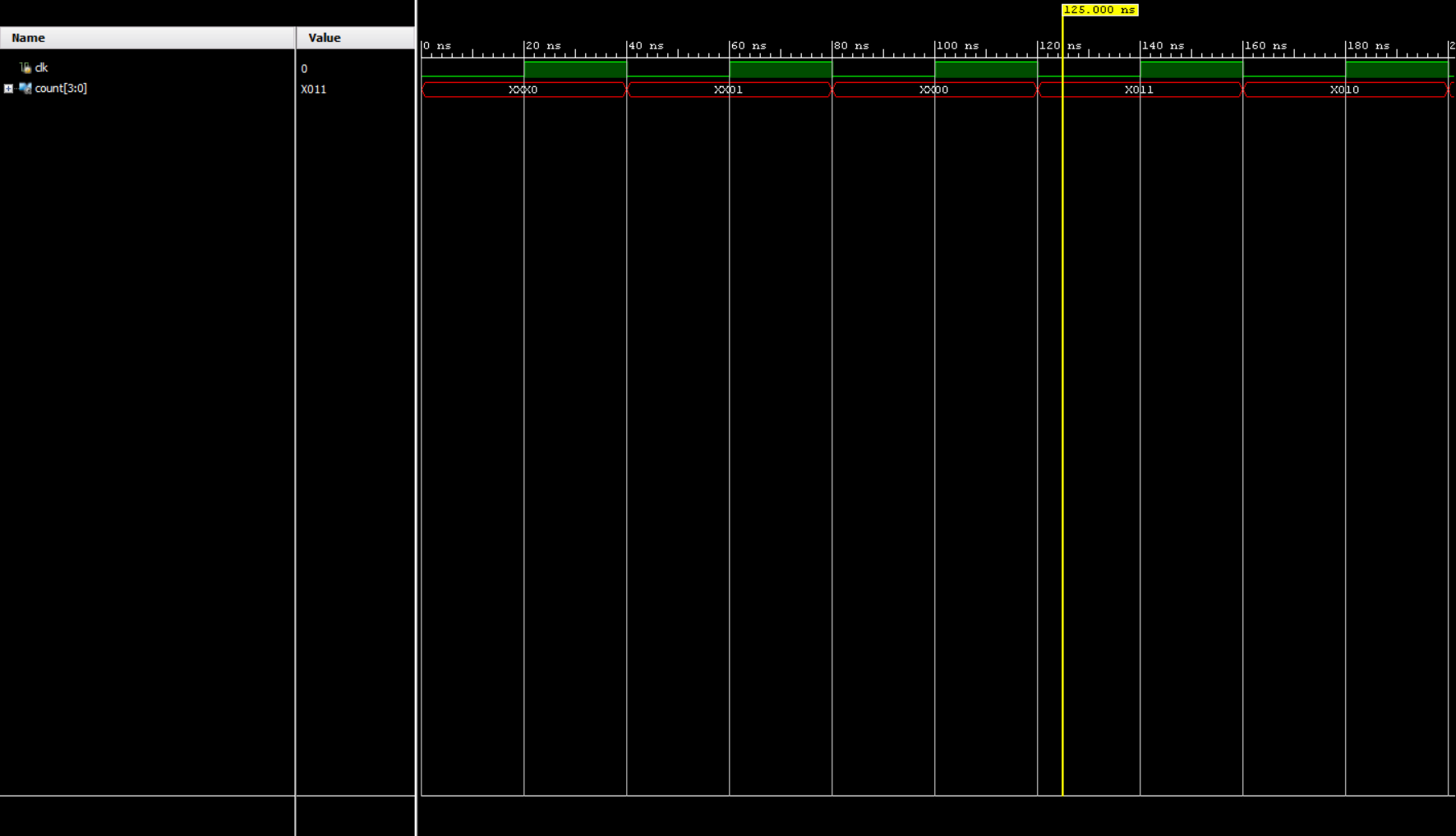


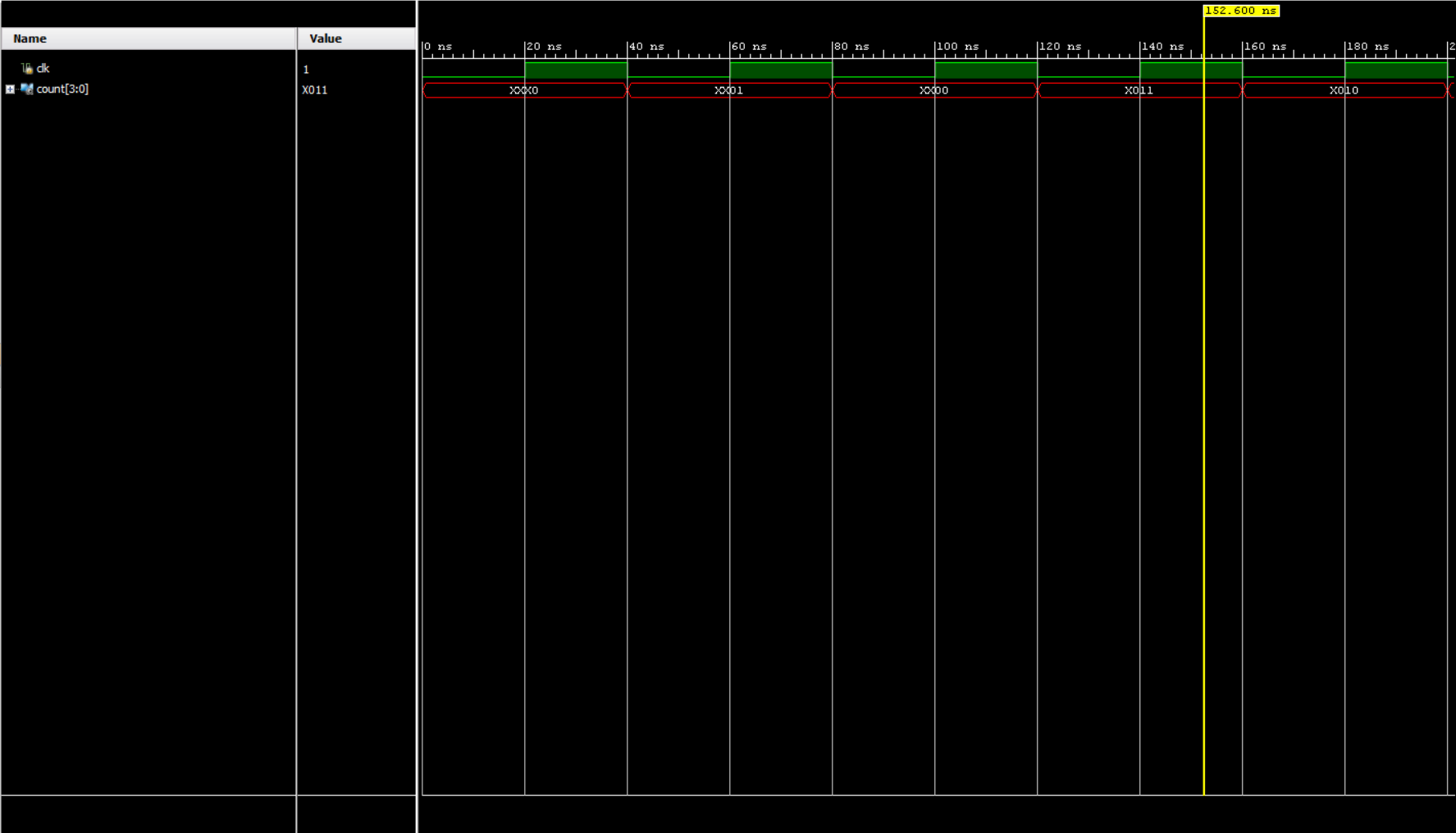


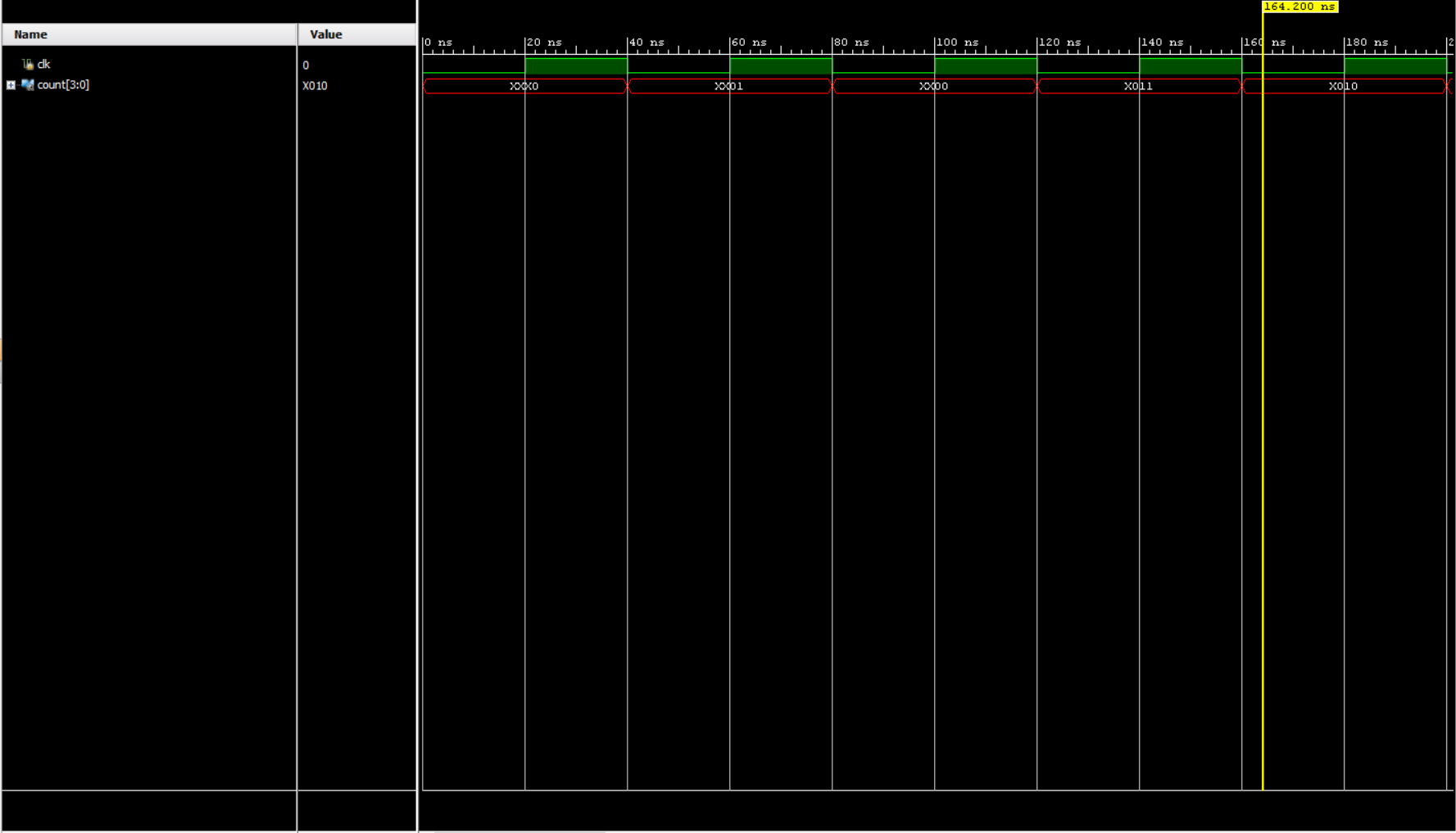


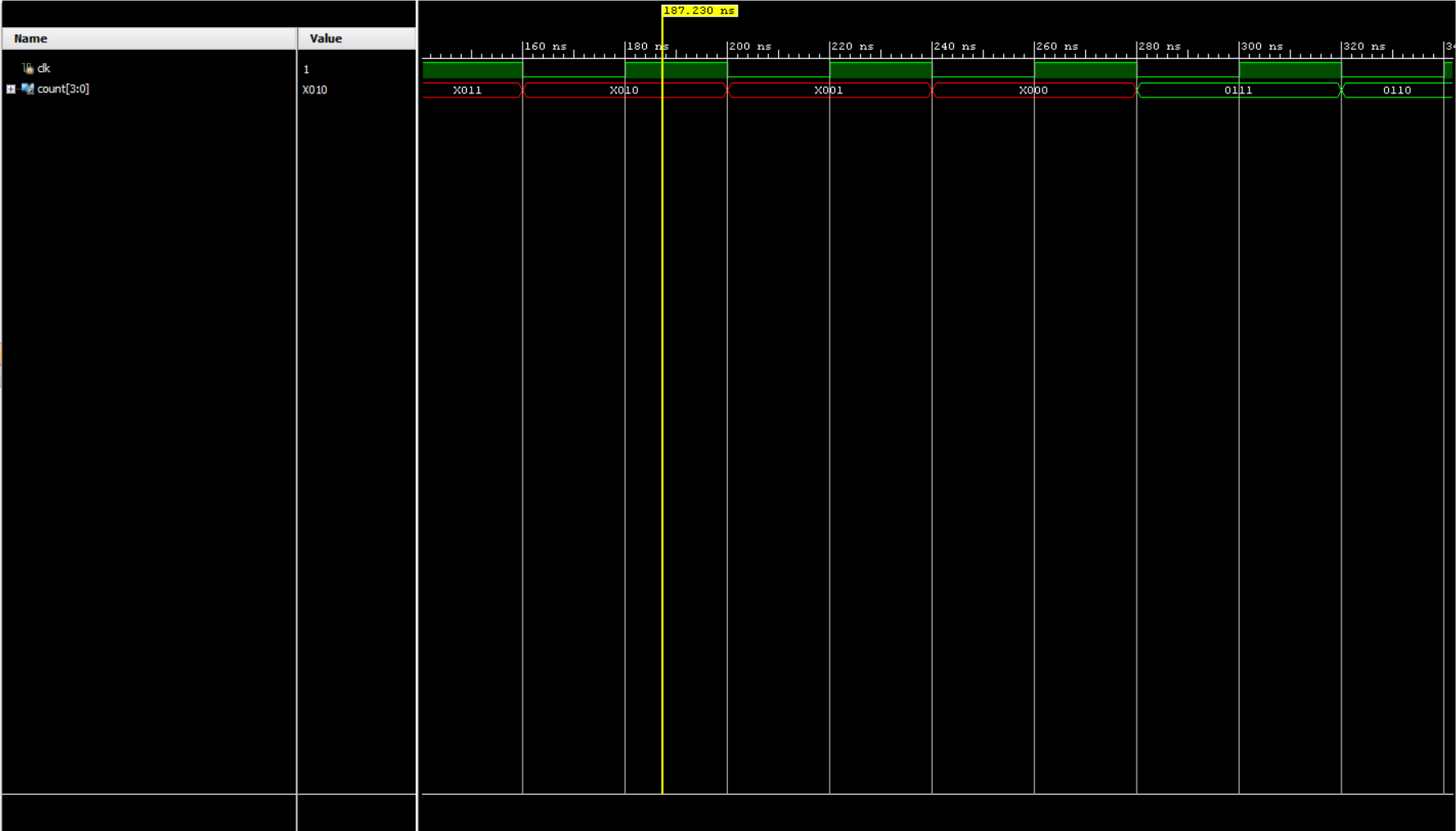


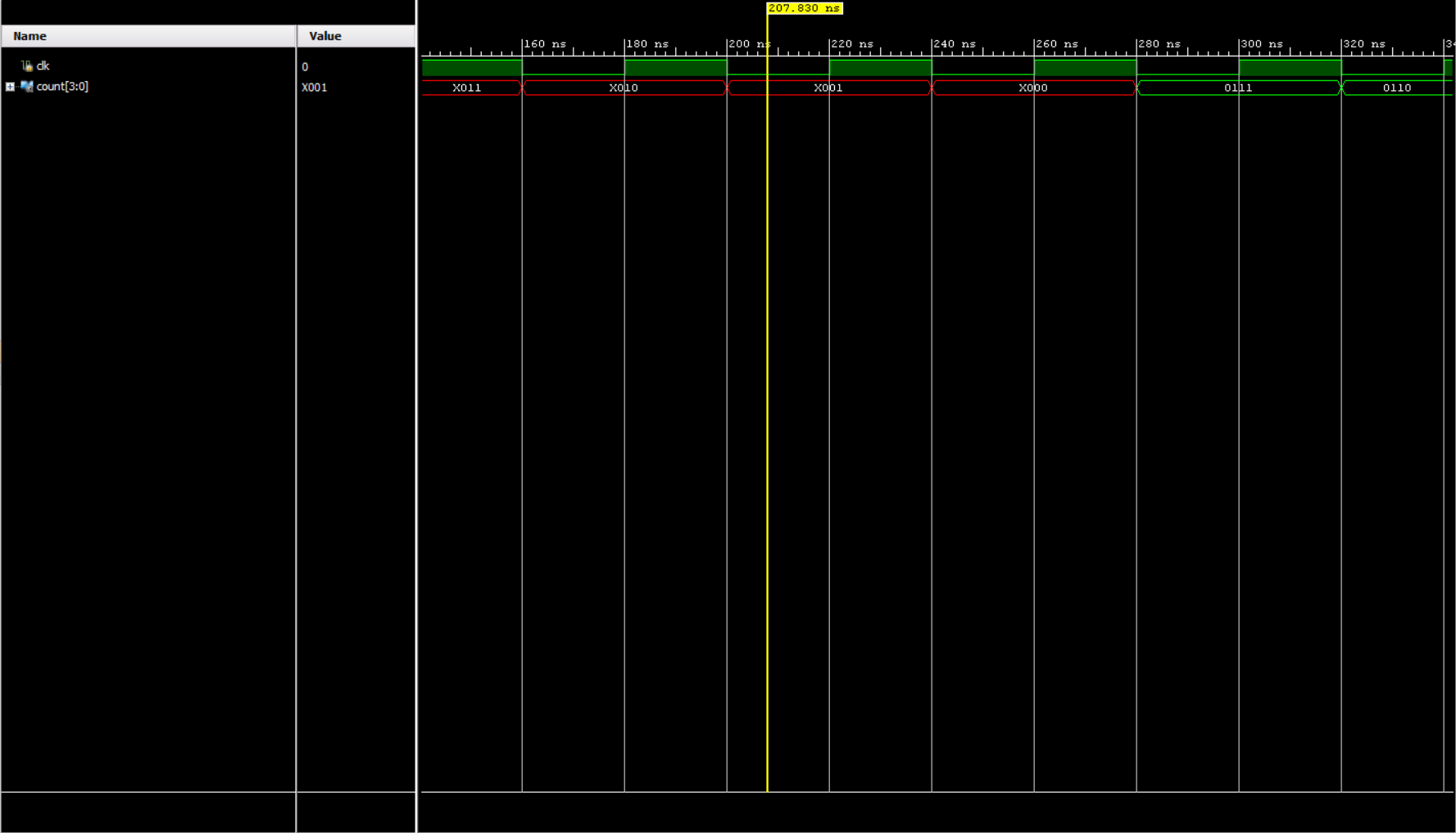


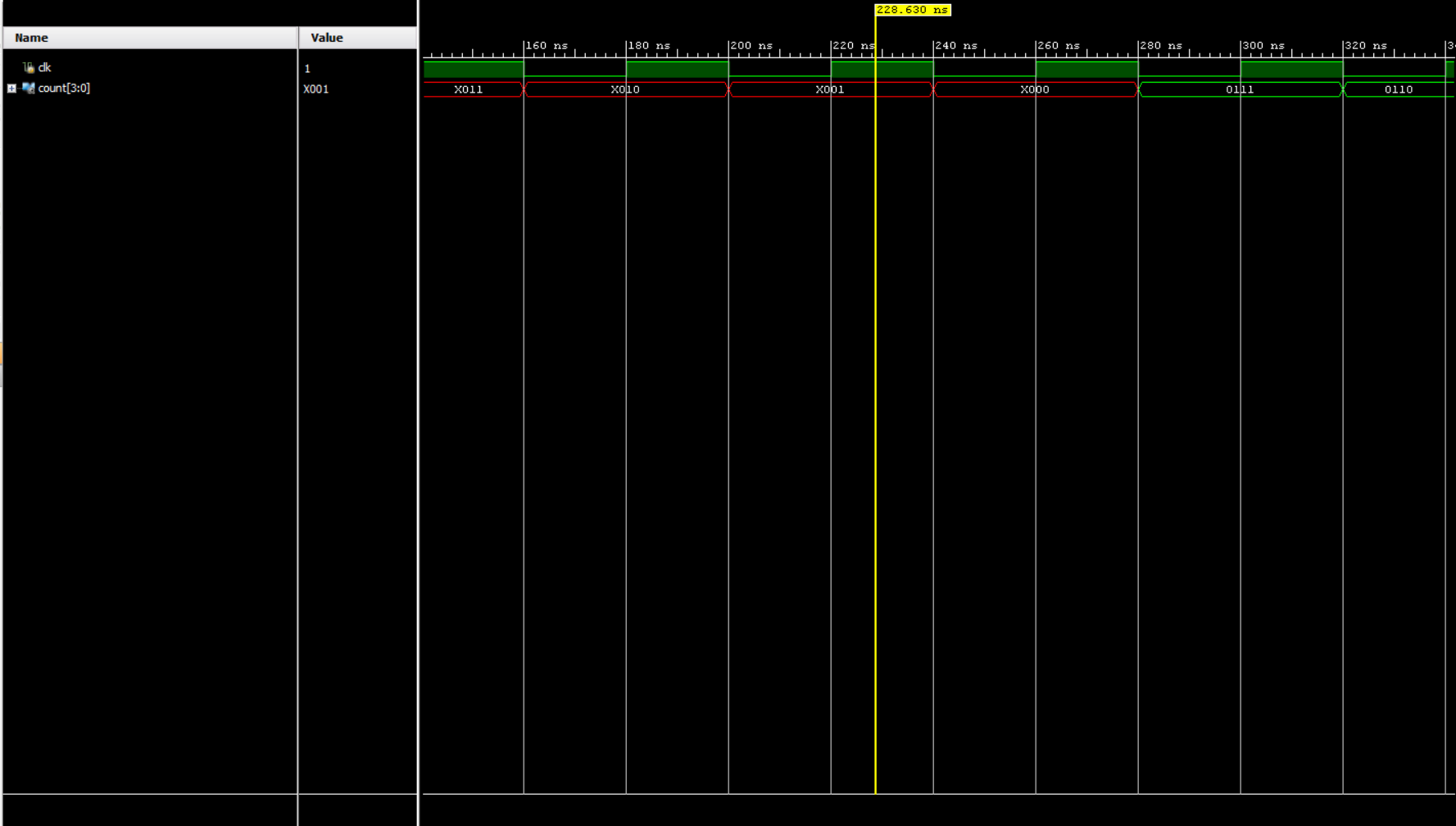


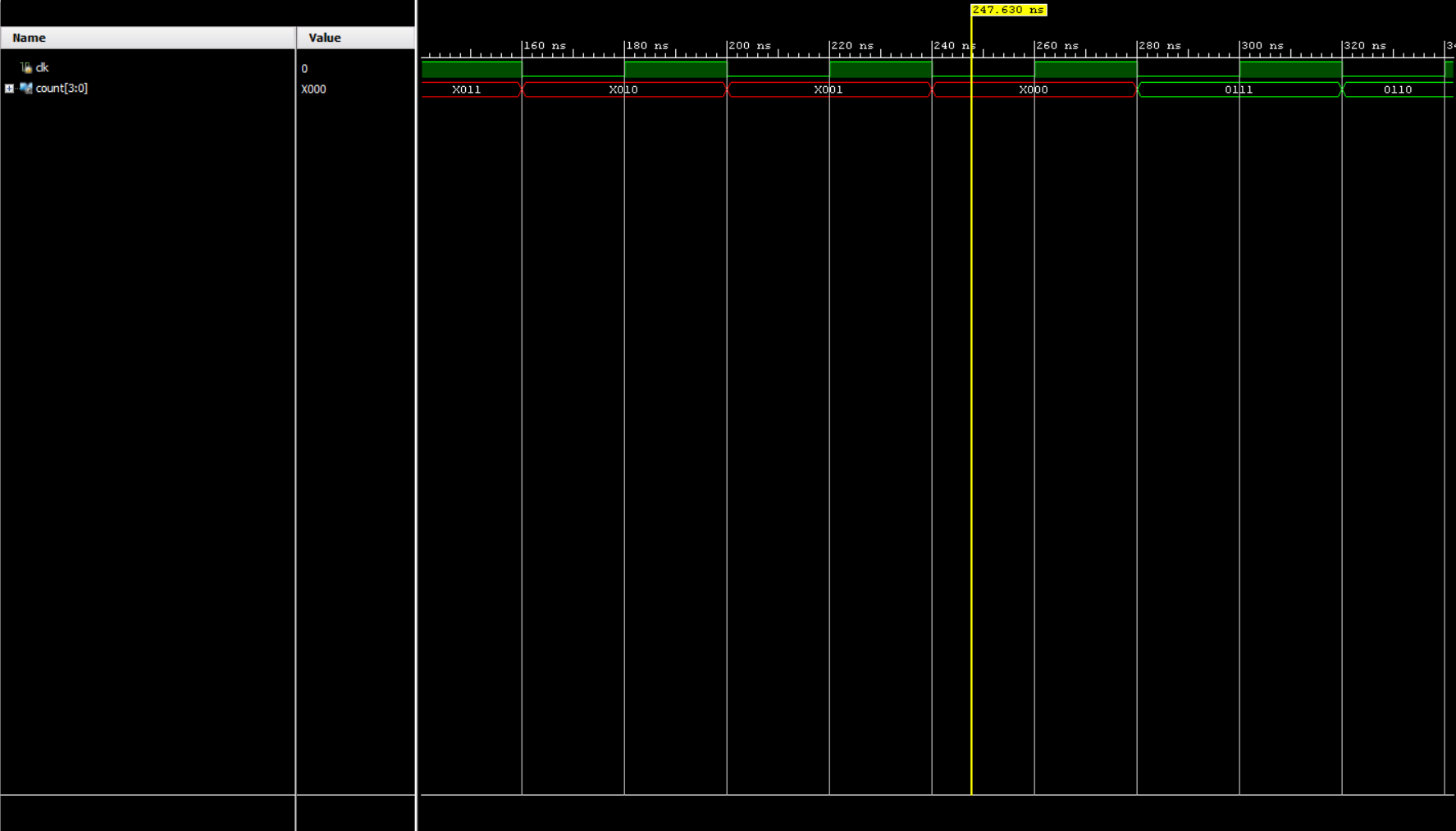




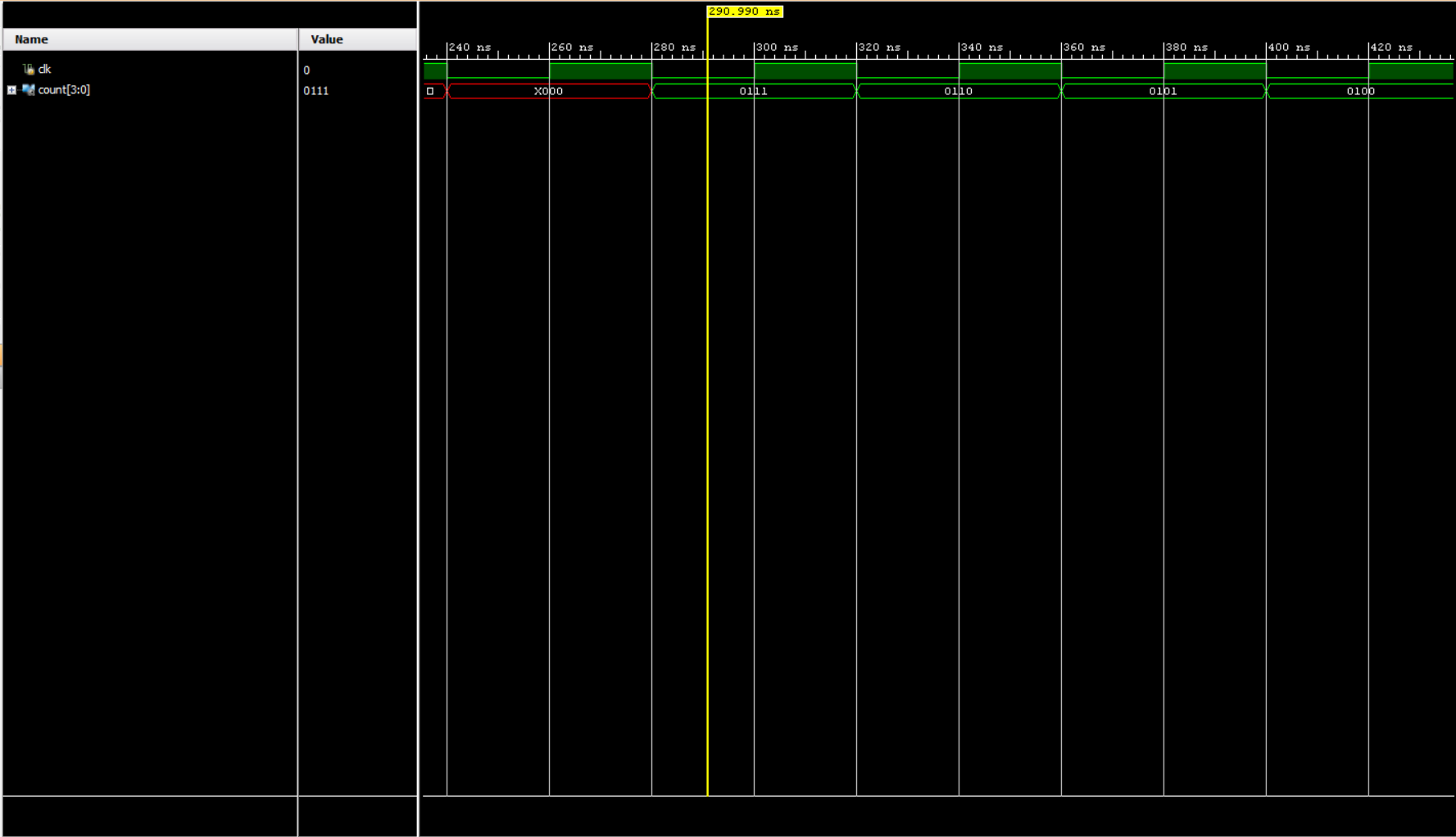


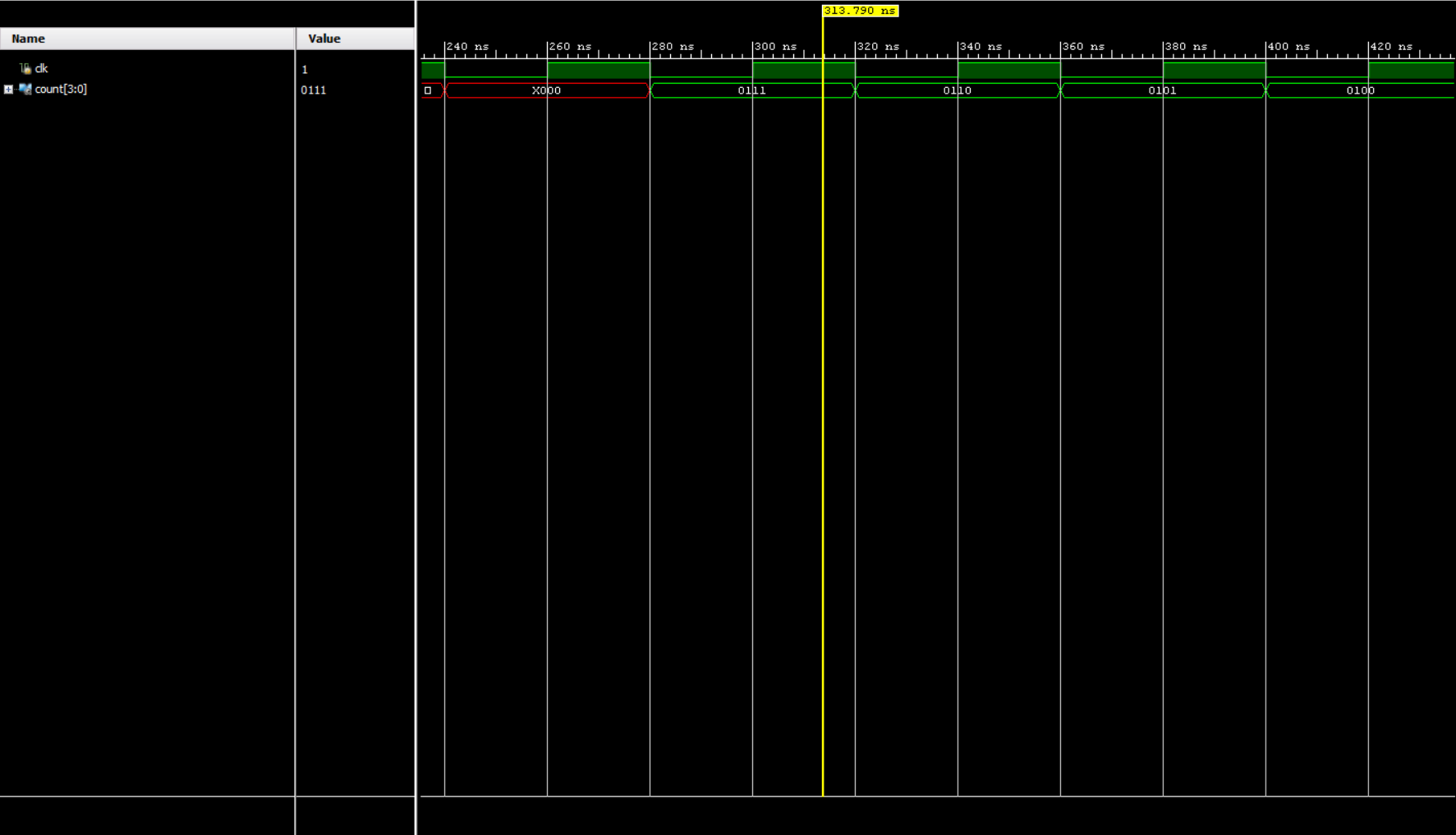


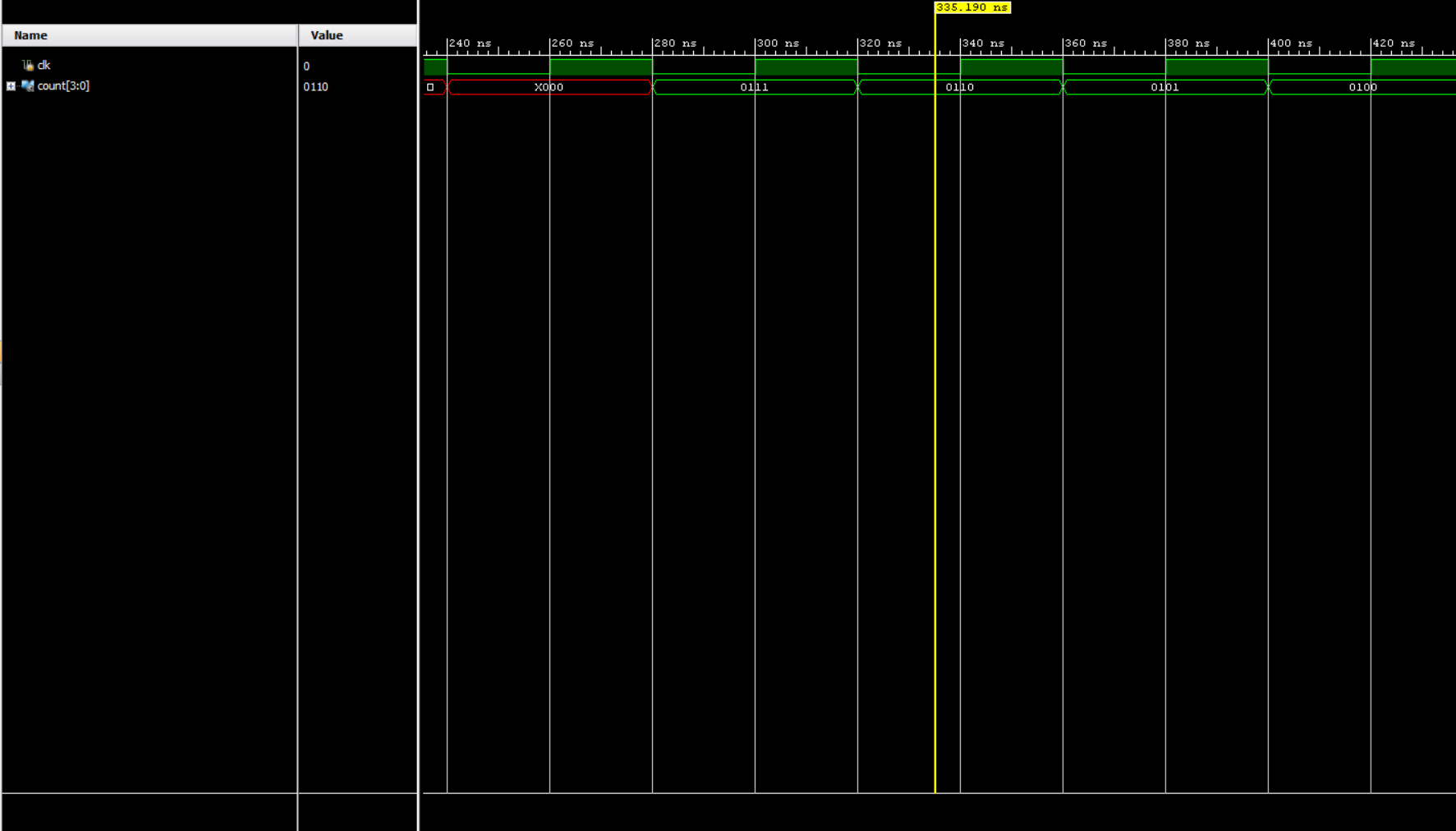












Conclusion:

The operation of down counter is exactly opposite to the up counter operation. Here every clock pulse at the input will reduce the count of the individual flip flop. So the down counter counts from 15, 14, 13…0 i.e. (0 to 1510) or 11112 to 00002.